

What Is Claimed Is:

1. A bus system produced by bundling several individual lines or buses or subbuses (see Figures 4, 5) within a unit of the DFP, FPGA or DPGA type as well as all units having a two- or multi-dimensional programmable cell architecture (see Figures 1, 2, 3) by means of which multiple units can be combined and/or memories and/or peripherals can be connected (see Figure 10).
2. The bus system according to claim 1, characterized in that one or more interfaces (Figures 6, 7) assume the function of combining the lines and create the bus system.
3. The bus system according to claim 1, characterized in that one or more state machines (0703/0603) control the interfaces (see Figures 6, 7).
4. The bus system according to claim 1, characterized in that the state machine also controls the external bus.
5. The bus system according to claim 1, characterized in that there is an address generator (0610/0710) which generates the addresses for the units to be contacted via the bus.
6. The bus system according to claim 1, characterized in that the interfaces use one or more internal bus systems which may comprise multiple lines (see Figures 4, 5) for reading and writing (see Figure 9a, I-BUS).
7. The bus system according to claim 1, characterized in that the interfaces use one or more internal bus systems which may comprise multiple lines (see Figures 4,

5) for either reading or writing (see Figure 9b, II-BUS, IO-BUS).

8. The bus system according to claim 1, characterized in that the interfaces operate one or more internal bus systems which may comprise multiple lines (see Figures 4, 5) in hybrid operation according to claims 6 and 7.

9. The bus system according to claim 1, characterized in that there is one register for managing and controlling the bus system (EB-REG 0702, 0602).

10. The bus system according to claim 1, characterized in that the bus is controlled by a unit (E-BUS MASTER) which accesses a plurality of lower-level units (E-BUS SLAVE).

11. The bus system according to claim 1, characterized in that the bus control is transferred dynamically from one unit (E-BUS MASTER) to another (MASTER record in EB-REG).

12. The bus system according to claim 1, characterized in that a lower-level unit (E-BUS SLAVE) can request the bus control (record of REQ-Master in EB-REG).

13. The bus system according to claim 1, characterized in that there is a register indicating whether data are stored in the interfaces (SET-REG, 0612, 0712).

14. The bus system according to claim 1, characterized in that the interfaces are either implemented directly on the unit or are created by the configuration of logic cells, i.e., cells in DFP, FPGA, DPGA or similar units which fulfill simple logical or arithmetic functions

according to their configuration.

15. The bus system according to claim 1, characterized in that the interfaces can be configured by a primary logic unit and/or the unit itself (see Figures 8, 11).

16. The bus system according to claim 1, characterized in that the primary logic unit is partially integrated on the unit.

17. The bus system according to claim 1, characterized in that standard bus systems can be used (see Figure 12).

18. The bus system according to claim 1, characterized in that the unit has additional ordinary connections in the manner customary with DFPs, FPGAs, DPGAs, etc. (see Figure 12 1201, 1204).